Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the above-identified application.

Listing of Claims

1. (Previously presented) A method comprising:

a memory circuit receiving a data frame to be subsequently transmitted to a destination device via a first or second switching fabric, wherein the data frame comprises header and data fields, and wherein the first switching fabric comprises data ports through which data frames enter or exit the first switching fabric, wherein the second switching fabric comprises data ports through which data frames enter or exit the second switching fabric;

selecting a first multi-bit value from a plurality of first multi-bit values according to the data contained in the one of the header fields, wherein the selected first multi-bit value comprises concatenated first and second multi-bit portions, wherein the bits of the first multi-bit portion correspond, respectively, to the data ports of the first and second switching fabrics, and wherein the bits of the second multi-bit portion correspond, respectively, to the data ports of the first and second switching fabrics;

selecting a second multi-bit value from a plurality of second multi-bit values according to the data contained in the one of the header fields, wherein the bits of the first multi-bit value correspond, respectively, to the data ports of the first and second switching fabrics;

concatenating the second multi-bit value with itself to produce a concatenated second multi-bit value;

bit wise logically ANDing the selected first multi-bit value with the concatenated second multi-bit value to produce a third multi-bit value, wherein the third multi-bit comprises concatenated first and second portions;

selecting one of the first and second portions of the third multi-bit value;

adding the selected one of the first and second portions of the third multi-bit value to another header field of the received data frame;

transmitting the received data frame from the memory circuit to one of the first and second switching fabrics;

the data frame exiting the one of the first and second switching fabrics through one or more data ports thereof in accordance with the values of the bits of the selected one of the first and second portions of the third multi-bit value.

2. (Original) The method of claim 1 wherein the memory circuit is coupled to the first and second switching fabrics via first and second data ports, respectively, wherein the first data port is one of the first switching fabric data ports and the second data port is one of the second switching fabric data ports.

3. (Original) The method of claim 2 wherein the data frame is transmitted to the first switching fabric via the first data port or the second switching fabric via the second data port.

4. (Original) The method of claim 1 wherein the destination device is coupled to the first and second switching fabrics via third and fourth data ports, respectively, wherein the third data port is one of the first switching fabric data ports and the fourth data port is one of the second switching fabric data ports.

5. (Original) The method of claim 4 wherein the data frame is transmitted from the first switching fabric to the destination device via the third data port or the data frame is transmitted from the second switching fabric to the destination device via the fourth data port.

6. (Original) The method of claim 1 wherein each bit of the second multi-bit value is set to logical 1 or logical 0, wherein each bit set to logical 1 corresponds, respectively, to one of the data ports of the first and second switching fabrics through which the data frame may exit to reach the destination device.

7. (Original) The method of claim 4 wherein each bit of the first and second portions of the first multi-bit value is set to logical 1 or logical 0, wherein each of the first and second portions of the first multi-bit value comprises a first bit that corresponds to the fourth data port, and wherein only one of the two first bits is set to logical 1.

8. (Original) The method of claim 1 wherein only one bit of the selected one of the first and second portions of the third multi-bit value is set to logical 1, and wherein the one bit corresponds to a particular data port of the first and second switching fabric ports through which the data frame must exit to reach the destination device.

9. (Original) An apparatus comprising:

a memory circuit configured to receive a data frame to be subsequently transmitted to a destination device via a first or second switching fabric, wherein the data frame comprises header and data fields, wherein the first switching fabric comprises data ports through which data frames enter or exit the first switching fabric, and wherein the second switching fabric comprises data ports through which data frames enter or exit the second switching fabric;

a first circuit coupled to the memory circuit, wherein the first circuit is configured to receive data from one of the header fields, and wherein the first circuit is configured to produce a first multi-bit value in response to receiving the data;

a second circuit coupled to the memory circuit, wherein the second circuit is configured to receive the data, and wherein the second circuit is configured to produce a second multi-bit value in response to receiving the data;

a third circuit coupled to the first and second circuits, wherein the third circuit is configured produce a third multi-bit value in response to receiving the first and second multi-bit values from the first and second circuits, respectively, wherein the third circuit is configured to add the third multi-bit to another header field of the data frame;

wherein the memory circuit is configured to transmit the data frame to the first or second switching fabric after the third multi-bit value is added to the header field;

wherein the third multi-bit value identifies one of the data ports of the first or second switching fabrics through which the data frame must exit the switching fabric to reach the destination device.

10. (Original) The apparatus of claim 9 wherein the memory circuit is coupled to the first and second switching fabrics via first and second data ports, respectively, wherein the first data port is one of the first switching fabric data ports and the second data port is one of the second switching fabric data ports.

11. (Original) The apparatus of claim 9 further comprising the first and second switching fabrics and the destination device, wherein the destination device is coupled to the first and second switching fabrics via third and fourth data ports, respectively, wherein the third data port is one of the first switching fabric data ports and the fourth data port is one of the second switching fabric data ports.

12. (Previously presented) The apparatus of claim 11 wherein each bit of the second multi-bit value is set to logical 1 or logical 0, wherein each bit set to logical 1 corresponds, respectively, to one of data ports of the first and second switching fabrics through which the data frame may exit to reach the destination device.

13. (Previously presented) The apparatus of claim 11 wherein the first multi-bit value comprises concatenated first and second multi-bit portions, wherein the bits of the first multi-bit portion correspond, respectively, to the data ports of the first and second switching fabrics, wherein the bits of the second multi-bit portion correspond, respectively, to the data ports of the first and second switching fabrics, wherein each of the first and second portions of the first multi-bit value comprises a first bit that corresponds to the fourth data port, and wherein only one of the two first bits is set to logical 1.

14. (Previously presented) The apparatus of claim 11 wherein the third circuit comprises a concatenation circuit and an ANDing circuit, wherein the concatenation circuit is configured to concatenate the second multi-bit value with itself to produce a concatenated second multi-bit value, and wherein the ANDing circuit is configured to bit wise logically AND the first multi-bit value with the concatenated second multi-bit value.

15. (Previously presented) The apparatus of claim 11 wherein only one bit of the third multi-bit value that is set to logical 1, and wherein the one bit corresponds to one data port of the first and second switching fabrics through which the data frame must exit to reach the destination device.

16. **(Currently amended)** An apparatus comprising:

a buffer configured to receive a first data frame and a second data frame to be transmitted to a destination device; ~~a data frame to be transmitted to a destination device via a first or second switching fabric, wherein the first switching fabric comprises data ports through which data frames enter or exit the first switching fabric, and wherein the second switching fabric comprises data ports through which data frames enter or exit the second switching fabric;~~

a routing data generation circuit coupled to the buffer, wherein the routing data generation circuit is configured to generate and add a first routing data to the first data frame ~~received by the buffer~~ , wherein the first routing data identifies a first data port of a first switching fabric ~~one of the data ports of the first or second switching fabric~~ through which the first data frame will exit to reach the destination device;

wherein the routing data generation circuit is configured to generate and add a second routing data to the second data frame, wherein the second routing data identifies a second data port of a second switching fabric through which the second data frame will exit to reach the destination device, and wherein the second data port is different from the first data port;

wherein the buffer is configured to transmit the ~~received~~ first data frame to the first switching fabric ~~at least one of the first and second switching fabrics~~ after the routing data generation circuit adds the first routing data to the first data frame; and ~~data frame.~~

wherein the buffer is configured to transmit the second data frame to the second switching fabric after the routing data generation circuit adds the second routing data to the second data frame.

17. (Canceled)

18. **(Currently amended)** An apparatus comprising:

a memory circuit configured to receive a first data frame and a second data frame to be transmitted to a destination device; ~~a data frame to be transmitted to a destination device via a first or second switching fabric, wherein the first switching fabric comprises data ports through which data frames enter or exit the first switching fabric, and wherein the second switching fabric comprises data ports through which data frames enter or exit the second switching fabric;~~

means coupled to the memory circuit, to generate and add a first routing data to the first data frame, wherein the first routing data identifies a first data port of a first switching fabric through which the first data frame will exit to reach the destination device; ~~routing data to the data frame received by the memory circuit, wherein the routing data identifies one of the data ports of the first or second switching fabric through which the data frame will exit to reach the destination device;~~

means coupled to the memory circuit, to generate and add a second routing data to the second data frame, wherein the second routing data identifies a second data port of a second switching fabric through which the second data frame will exit to reach the destination device, and wherein the second data port is different from the first data port;

wherein the memory circuit is configured to transmit the first data frame to the first switching fabric after the first routing data has been added to the first data frame; and ~~received data frame to at least one of the first and second switching fabrics after the means adds the routing data to the data frame.~~

wherein the memory circuit is further configured to transmit the second data frame to the second switching fabric after the second routing data has been added to the second data frame.

19. (Canceled)

20. **(Currently amended)** A method comprising:

~~a memory circuit~~ receiving a first data frame and a second data frame to be transmitted to a destination device; ~~a data frame to be transmitted to a destination device via first or second switching fabrics, wherein the first switching fabric comprises data ports through which data frames enter or exit the first switching fabric, and wherein the second switching fabric comprises data ports through which data frames enter or exit the second switching fabric;~~

generating and adding a first routing data to the first data frame ~~received by the memory circuit~~ , wherein the first routing data identifies a first data port of a first switching fabric ~~one of the data ports of the first or second switching fabric~~ through which the first data frame will exit to reach the destination device;

generating and adding a second routing data to the second data frame, wherein the second routing data identifies a second data port of a second switching fabric through which the second data frame will exit to reach the destination device, and wherein the second data port is different from the first data port;

~~the memory circuit~~ transmitting the ~~received~~ first data frame to the first switching fabric ~~at least one of the first and second switching fabrics~~ after the first routing data has been added to the first data frame; and ~~data frame.~~

transmitting the second data frame to the second switching fabric after the second routing data has been added to the second data frame.

21. **(Currently amended)** A computer readable medium storing instructions executable by a computer system to implement a method, the method comprising:

~~a memory circuit of the computer system~~ receiving a first data frame and a second data frame to be transmitted to a destination device; ~~a data frame to be transmitted to a destination device via first or second switching fabrics, wherein the first switching fabric comprises data ports through which data frames enter or exit the first switching fabric, and wherein the second switching fabric comprises data ports through which data frames enter or exit the second switching fabric;~~

generating and adding a first routing data to the first data frame ~~received by the memory circuit~~ , wherein the first routing data identifies a first data port of a first switching fabric ~~one of the data ports of the first or second switching fabric~~ through which the first data frame will exit to reach the destination device;

generating and adding a second routing data to the second data frame, wherein the second routing data identifies a second data port of a second switching fabric through which the second data frame will exit to reach the destination device, and wherein the second data port is different from the first data port;

~~the memory circuit~~ transmitting the ~~received~~ first data frame to the first switching fabric ~~at least one of the first and second switching fabrics~~ after the first routing data has been added to the first data frame; and ~~data frame.~~

transmitting the second data frame to the second switching fabric after the second routing data has been added to the second data frame.

22. **(Currently amended)** The apparatus of claim 16, wherein the routing data generation circuit is configured to generate the first routing data ~~generates the routing data~~ as a function of:

a port data set, wherein the port data set identifies one selected data port for each of a plurality of devices coupled to at least one of the first and second switching fabrics; and

a destination data set, wherein the destination data set identifies each available data port coupled to a set of destination devices among ~~selected from~~ the plurality of devices.

23. **(Currently amended)** The apparatus of claim 22,

wherein the port data set comprises a set of port bits, wherein each port bit corresponds to a data port coupled to the plurality of devices and indicates a selection or non-selection of the corresponding data port; and

wherein the destination data set comprises a set of device bits, wherein each device bit corresponds to a data port coupled to the plurality of devices and indicates a selection or non-selection of a corresponding device.

24. **(Currently amended)** The apparatus of claim 18, wherein the means coupled to the memory circuit is configured to generate the first routing data ~~generates the routing data~~ as a function of:

a set of port bits, wherein the set of port bits identifies one selected data port for each of a plurality of devices coupled to at least one of the first and second switching fabrics, and wherein each port bit corresponds to a data port coupled to the plurality of devices and indicates a selection or non-selection of the corresponding data port; and

a set of device bits, wherein the set of device bits identifies each available data port coupled to a set of destination devices among ~~selected from~~ the plurality of devices, and wherein each device bit corresponds to a data port coupled to the plurality of devices and indicates a selection or non-selection of a corresponding device.

25. **(Currently amended)** The method of claim 20, wherein the first routing data are generated as a function of:

a port data set, wherein the port data set identifies one selected data port for each of a plurality of devices coupled to at least one of the first and second switching fabrics; and

a destination data set, wherein the destination data set identifies each available data port coupled to a set of destination devices among ~~selected from~~ the plurality of devices.

26. **(Currently amended)** The computer readable medium of claim 21, wherein the first routing data are generated as a function of:

a port data set, wherein the port data set identifies one selected data port for each of a plurality of devices coupled to at least one of the first and second switching fabrics; and

a destination data set, wherein the destination data set identifies each available data port coupled to a set of destination devices among ~~selected from~~ the plurality of devices.

27. **(New)** An apparatus comprising:

a buffer configured to receive a data frame to be transmitted to a destination device via a first or second switching fabric, wherein the first switching fabric comprises data ports through which data frames enter or exit the first switching fabric, and wherein the second switching fabric comprises data ports through which data frames enter or exit the second switching fabric; and

a routing data generation circuit coupled to the buffer, wherein the routing data generation circuit is configured to generate and add routing data to the data frame received by the buffer, wherein the routing data identifies one of the data ports of the first or second switching fabric through which the data frame will exit to reach the destination device;

wherein the buffer is configured to transmit the received data frame to at least one of the first and second switching fabrics after the routing data generation circuit adds the routing data to the data frame;

wherein the routing data generation circuit is configured to generate the routing data as a function of:

a port data set, wherein the port data set identifies one selected data port for each of a plurality of devices coupled to at least one of the first and second switching fabrics, and

a destination data set, wherein the destination data set identifies each available data port coupled to a set of destination devices among the plurality of devices.

28. **(New)** A method comprising:

receiving a data frame to be transmitted to a destination device via first or second switching fabrics, wherein the first switching fabric comprises data ports through which data frames enter or exit the first switching fabric, and wherein the second switching fabric comprises data ports through which data frames enter or exit the second switching fabric;

generating and adding routing data to the data frame received by the memory circuit, wherein the routing data identifies one of the data ports of the first or second switching fabric through which the data frame will exit to reach the destination device; and

transmitting the received data frame to at least one of the first and second switching fabrics after the routing data has been added to the data frame;

wherein the routing data are generated as a function of:

a port data set, wherein the port data set identifies one selected data port for each of a plurality of devices coupled to at least one of the first and second switching fabrics, and

a destination data set, wherein the destination data set identifies each available data port coupled to a set of destination devices among the plurality of devices.

29. **(New)** The method of claim 20, further comprising:

selecting the first switching fabric for a first data flow comprising the first data frame; and

selecting the second switching fabric for a second data flow comprising the second data frame.

30. **(New)** The method of claim 29,

wherein the selecting the first switching fabric for the first data flow comprises a random selection of a switching fabric; and

wherein the selecting the second switching fabric for the second data flow comprises a random selection of a switching fabric.